ABSTRACT OF THE DISCLOSURE

A parallel decoder, which is simpler and more flexible than conventional devices, is provided in decoding device for a LDPC code. The present invention includes a plurality of memory units for storing a received value and a message generated during a Message-Passing decoding, a plurality of variable node function units, a plurality of check node function units, a plurality of address generation units for generating an address of each of memory units, and a plurality of shuffle network units for determining a connection between variable node function units and check node function units. An address generation unit generates an address on the basis of a plurality of permutations. Each shuffle network unit is connected to some of the variable node function units. This connection is determined on the basis of a plurality of permutations. A change of the permutations in the address generation units and a change of the permutations in the shuffle network units are performed in the same cycle in a decoding process.